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Original Article

Voltage Over Scaling Based GDI Approximate Adder

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Abstract - *Machine Learning (ML) models are deployed in resource-constrained edge and fog devices in the Internet of Things (IoT) paradigm. The ML models are trained with Convolutional Neural Networks (CNN) which directly influence the device performances like power, speed, and network bandwidth. In such cases, efficient hardware devices are needed to implement the ML models. This work aims to identify performance-efficient techniques and adapt them to the proposed design. This paper proposes Voltage Over Scaling (VOS) based Gate Diffusion Input (GDI) Approximate Full Adder (AFA) identified as VOS-GAFA at the transistor level. The proposed VOS-GAFA is used to develop the 8-bit VOS-based Ripple Carry Adder (RCA) identified as VOS-RCA. The experimental results of the proposed VOS-GAFA have shown 56.11 % and 44 % reduction of power consumption and transistor count, respectively, when compared to the best existing approximate full adder. Moreover, VOS-GAFA has a high Noise Margin (NM) value that provides proper circuit operation and robustness against noise sources. VOS-RCA showed improved power, PDP, and delay values when compared to existing 8-bit RCA, and hence, it is appropriate for resource-constrained edge and fog IoT devices. This research work is carried out using the cadence virtuoso tool at gpdk45nm technology.*

Keywords - *Approximate computing, Gate diffusion input, Low power full adder, Machine Learning, Voltage over scaling.*

1. Introduction

By 2027 [1], there will be more than 30 billion IoT devices, hence posing a challenge to the capacity of cloud computing since the device relies on data offloading for processing [2], which increases data transfers between IoT devices and the cloud. This increases computation power, network bandwidth and energy consumption. In addition, this forces the data centres to handle unexpected rises in the number of user requests. To address the increased processing power, network bandwidth, and energy consumption, Edge and Fog computing were created [3] in the IoT paradigm, as well as smart sensing and wearability, autonomous driving, and positioning.

The Edge and fog computing are detailed in [5-8], and it provides the following advantages:

- Minimizing data transfer to the cloud results in decreased communication bandwidth and power consumption.
- Real-time processing of data.
- Increases security due to the processing of data on the edges.
- Increases the reliability due to distributed computing.

Integrated Circuits (ICs) play an important role in advanced devices like mobile phones, motivating researchers to develop and optimize these devices. Arithmetic circuits such as multipliers, compressors, and Full Adders (FA) are essential in digital circuitry for numerical computations. The digital counters, as an arithmetic circuitry, were regarded as inadequate for other circuits. The compressing capability of countercircuits was advantageous in the development of multipliers [6]. In designing digital circuits, particularly in counters, power consumption, latency, and area occupancy are essential characteristics. Decreasing the voltage provided to the circuit layers is an efficient strategy for minimizing dynamic power. This also stipulates the criteria for restoring the applied voltage to nominal levels through the Level Shifter (LS) circuits and VOS technique. The supply voltage may be increased while preserving consistent performances if the system can accommodate timing inaccuracies [7].

The VOS is utilized for the Approximate Computing (AxC) circuits with a focus on their error tolerance. Nonetheless, the VOS could enhance the efficacy of error-free (accurate) circuits. The implementation of VOS enhances energy efficiency, longevity, and dependability. Conversely, the implementation of the VOS in the circuits exacerbates their delay, particularly affecting key path delays more significantly.

Consequently, integrating the aforementioned methods is advantageous for achieving a low-power, high-speed circuit with full-swing and drivability outputs [8]. Various strategies have been suggested to minimize switching activity, frequency, or supply voltage of the circuit to lower power

consumption. The best approach to reduce power consumption is VOS, mostly because of the quadratic relationship between dynamic power usage and supply voltage. VOS expands the principle of voltage scaling above the critical voltage threshold at which the critical delay in the path (clock period) dictated by design and application is adequately maintained [9]. VOS could result in substantial energy conservation; however, it adversely affects performance and increases the circuit's susceptibility to noise. VOS specifically contributes to delays in all computational pathways, potentially resulting in erroneous operation calculations and significantly diminishing output quality. The implementation of VOS is additionally difficult as it raises both the mean delay (μ) and the standard deviation (σ) of the distribution of total path delay [10].

1.1. Problem Statement & Research Gap

The increasing demand for low-power, high-performance, and energy-efficient arithmetic circuits has led to the adoption of approximate computing techniques in various applications such as IoT, AI, multimedia, and image processing. However, existing approximate FAs and RCAs often suffer from trade-offs between power, delay, energy efficiency, and transistor count, limiting their applicability in resource-constrained and error-tolerant scenarios.

While techniques like GDI, VOS, and Negative Capacitance FET have demonstrated improvements in specific metrics, issues such as high power consumption, high delay, threshold voltage drops, and application-specific focus persist. Additionally, most studies lack a comprehensive evaluation of these adders in terms of Power-Delay-Product (PDP) efficiency and their impact on large-scale systems like RCAs under different process corners. This research addresses the gap by proposing and analyzing novel approximate computing designs with optimized power, delay, PDP, and transistor efficiency, targeting a balanced trade-off suitable for real-world error-tolerant applications.

Hence, it is important to design efficient edge and fog computing devices, which opens the opportunity for researchers to develop new low-power-energy efficient intelligent devices. In computing, an adder is the fundamental block that is frequently used and large in numbers. Hence, the adder has a direct impact on the performance of devices. Therefore, it is necessary to optimize the adder to improve the performance metrics.

The purpose of this work is to discuss techniques that provide power, delay, and area efficiency and then adapt the efficient methodologies for the design and development of adders. There are several techniques, including VOS, different logic styles, clock gating, power gating, Multi-threshold CMOS, adaptive body biasing, sub-threshold operation, and many are proposed for low-power design. Among these, VOS and GDI logic styles are discussed in this paper. Hence, the objective of this research is to design and develop approximate adders using VOS and GDI for resource-constrained hardware devices. This research introduces a novel VOS-GAFA with optimized power, delay, PDP, and transistor count, providing a balanced trade-off for efficient operation in error-tolerant applications.

The paper has the following sections. Section 2, briefs about AxC, VOS and GDI techniques. The design of the proposed 1-bit VOS-GAFA and 8-bit VOS-RCA is provided in Section 3. In Section 4, results and discussion are provided. Section 5 concludes the article.

2. Literature Review

This section briefly provides the related works of the proposed research. Authors in [5] provided a detailed review of AxC in edge IoT and AI applications. The authors discussed AxC at the circuit-level, architecture-level, application-level and algorithmic-level techniques and showed AxC applications in autonomous driving, smart sensing wearables and positioning. Moreover, the authors provided the future directions of AxC in the edge computing framework. In [9], authors proposed two GDI-MUX-based AFA adders, namely GMAFA1 and GMAFA2, and simulated them at a Vdd of 0.9V. The power, delay and PDP were high in both the adders. The Negative Capacitance FET (NCFET) based 6T-SRAM Computing-in-Memory (CiM) accurate full adder and reconfigurable CiM NCFET 6T-SRAM accurate as well as approximate full adder was proposed in [10] at 40nm bulk CMOS technology and Vdd of 0.5V. The NCFET-CiM has the best power, delay, and PDP efficiency; however, the transistor count was very high.

In [11], authors implemented 8-T approximate full adder, inexact subtractor and RCA at 32nm CNFET technology and Vdd of 0.9V. Here, the power, delay and PDP were high. Sadeghi et al. [12] proposed GDI and Dynamic Threshold (DT) based full adder in CNFET technology and simulated at 32nm CNFET technology with Vdd of 0.9V. This adder has high power, delay and PDP. The work in [13] proposed a Timing-Aware Configurable Adder (TACA) with Accuracy-Configurable Full Adders (ACFAs) at SMIC 40nm technology and Vdd of 0.5V.

The authors have demonstrated TACA-ACAFA in image processing and CNN-based classifications. This adder has low power, less delay and minimum PDP efficiency at the cost of very high transistor count. In [14], authors discussed the applications of GDI approximate adders in multimedia applications. Authors in [15] proposed Self-Adjusting Multi-Cycle Approximate Adders (SAMA and SAMA-F) and evaluated their performance at the supply voltage of 1.25V. The consumption of power and area were high in this technique because of the inclusion of controller logic. In [16], authors proposed approximate adders AA1, AA2, AA3 and AA4 for DSP processors. All adders provided extremely low

power consumption. However, the delay and PDP were very high. Static Approximate Adders (SPA) for FPGA, ASIC and FPGA-ASIC platforms were proposed in [17] at 32nm CMOS technology with a Vdd of 1.05V. The three HOAANED, HERLOA and M-HERLOA SPAs provided better Peak Signal-to-Noise Ratio (PSNR) and Structural Similarity Index Metric (SSIM) than others. However, the power consumption of the above three SPAs was high.

The author in [18] discussed different logic styles like TG, DPL, TG, and PTL and their issues. To solve the issues in these logic styles, the authors proposed GDI as the efficient logic design style to improve power and performance. The main problem in GDI was the threshold voltage drop in output. In [19], Modified GDI (MGDI) was presented to solve the threshold voltage drop problem in GDI. The authors in [22] discussed the deployment of GDI in Quantum dots Cellular Automata (QCA) and CNFET technologies. Authors in [23] proposed a synthesizable GDI library function. Recently, the work in [24] proposed a GDI reversible full adder using CNFET technology. VOS is the technique used in low-power design. The authors in [26] discussed the VOS-based Significance-Driven Computation (SDC) technique at an algorithmic level in approximate computing. The VOS-based low-power SDC was tested in motion estimation hardware for video encoding applications.

The results showed the power savings at different VOS levels. In [27], VOS-based approximate operators were proposed for error-tolerant applications. The authors demonstrated the implementation of VOS-based 8 and 16-bit Ripple Carry Adder (RCA) and Brent-Kung Adder (BKA), respectively. The results showed the energy efficiency when supply voltages were scaled from 1.0V to 0.4V. Discussed VOS at the circuit level approximate computing in [28] and pointed out that VOS provides low power consumption with allowable errors. Junqi Huang et al. [30] presented approximate computing using VOS for image processing applications. The results showed the Approximate Adders (AMA1) sustained lower supply voltages, consumed less energy at the reduced error rate, and had higher PSNR values compared to the exact full adder.

Table 1. Critical analysis of reviewed current works

Ref	Model	Advantages	Disadvantages
[5]	Reviewed AxC techniques at various levels (circuit, architecture, application, and algorithmic).	Comprehensive review of AxC and future directions.	No implementation or performance validation.
[9]	Proposed GDI-MUX-based AFAs (GMAFA1 and GMAFA2).	Innovative GDI-MUX-based design.	High power, delay, and PDP.
[10]	NCFET 6T-SRAM CiM accurate and approximate full adders.	Best power, delay, and PDP efficiency.	High transistor count.
[11]	Implemented 8-T approximate full adder, inexact subtractor, and RCA in CNFET technology.	Compact transistor design.	High power, delay, and PDP.
[12]	GDI and DT-based full adder in CNFET technology.	Use of dynamic threshold for optimization.	High power, delay, and PDP.
[13]	TACA-ACFA with accuracy-configurable adders.	Low power, less delay, and minimum PDP.	Very high transistor count.
[14]	Discussed GDI approximate adders.	Specific focus on multimedia use.	No detailed performance metrics were provided.
[15]	Self-Adjusting Multi-Cycle Approximate Adders (SAMA and SAMA-F).	Adaptive multi-cycle design.	High power and area due to controller logic.
[16]	Proposed AA1, AA2, AA3, and AA4 for DSP processors.	Extremely low power consumption.	Very high delay and PDP.
[17]	Static approximate adders (SPA) for FPGA, ASIC, and hybrid platforms.	Improved PSNR and SSIM in results.	High power consumption.
[18]	Reviewed TG, DPL, TG, and PTL logic styles and proposed GDI.	Efficient power and performance improvements.	Threshold voltage drop issue in GDI.
[19]	Modified GDI (MGDI) is used to address the GDI threshold voltage drop.	Solves the threshold voltage drop issue.	No detailed performance analysis was provided.

[22]	Deployment of GDI in QCA and CNFET technologies.	Applicability of GDI in emerging technologies.	No implementation results.
[23]	Proposed synthesizable GDI library function.	Simplified GDI usage through libraries.	Limited to library-specific scope.
[24]	Proposed GDI reversible full adder using CNFET technology.	VOS-based design for low power.	Limited performance comparison.
[26]	VOS-based SDC for motion estimation in video encoding.	Power savings at different VOS levels.	Application-specific focus.
[27]	VOS-based 8 and 16-bit RCAs and BKAs.	Energy-efficient operation at scaled supply voltages.	Limited to specific adder designs.
[28]	Discussed VOS at the circuit level for AxC.	Low power consumption with allowable errors.	No specific application or design details.
[29]	Approximate computing using VOS for image processing.	Lower energy consumption, reduced error rates, and higher PSNR.	Limited to specific adders (AMA1).

From the literature review discussions, it is clear that (i) the GDI technique improves performance and reduces active and leakage power, and (ii) the VOS technique reduces power consumption. Hence, this article utilizes the GDI and VOS techniques in approximate adder design. This article proposes that VOS-based GDI-AFA operate in scaled supply voltage. Then, 8-bit RCA is developed using VOS-GAFA.

3. Materials and Methods

3.1. Approximate Computing (AxC)

Approximate computing in digital design seeks to alleviate the necessity for precise computations to provide significant enhancements in power, speed, and space efficiency. Designers have consistently sought to reduce resource requirements by selecting the minimal bit-width and by simulating intricate operations.

The systematic study of approximate circuits for errors-resilient applications like multimedia processing, image processing, ML, and data mining, particularly in edge or embedded systems with stringent energy and speed limitations, is a relatively recent development. Approximate computing has been utilized in binary multipliers, binary divisions, MAC units, and complete systems. The FA serves as a fundamental component in arithmetic circuits, including adders, multipliers, and divisions. Numerous studies have introduced different iterations of approximation full adders and utilized them across numerous application domains.

The major motivation for approximation computing is error-tolerant applications. Approximate computing is defined as a software or hardware program that performs calculations with errors at an acceptable level [9-17]. As a result, it provides increased power, delay, and area efficiency. Error resilience of up to (≈83%) has been shown in a study by Chippaet et al. [31]. It is widely utilized in a variety of domains, including machine learning, deep learning, information analytics, scientific computing, and multimedia applications. The majority of works on approximate computing have been presented at the hardware level, particularly on arithmetic operations such as addition, subtraction and multiplication. Among this addition is the fundamental operation that is often used by several blocks. Hence, the addition operations directly influence the performance metrics. The AxC design methodologies, error characteristics and performance metrics of AxC adders were detailed in [9-17].

The Truth Table (TT) for the precise FA is presented in Table 2. The inputs are a, b, and c_{in}, whereas the outputs for sum and carry were denoted as s and c_o. The numerical sum of the inputs is denoted as 'S', and each element in the TT was indexed by i, which ranges from 0 (for $\{c_{in}, a, b\} = \{0,0,0\}$) to 7 (for $\{c_{in}, a, b\} = \{1,1,1\}$). The logical calculations of the FA are presented as follows:

$$s = a \oplus b \oplus c_{in} \quad (1)$$

$$c_o = ab + ac_{in} + bc_{in} \quad (2)$$

The expressions of s and c_o can be modified by complementing some of the TT's entries.

Table 2. TT of approximate FA

i	c_{in}	a	b	c_o	s
0	0	0	0	0	0
1	0	0	1	0	1
2	0	1	0	0	1
3	0	1	1	1	1
4	1	0	0	1	1
5	1	0	1	1	0
6	1	1	0	1	0
7	1	1	1	1	0

Table 3. TT of approximate FA similar to table 1

i	c_{in}	a	b	c_o	s
0	0	0	0	0	0
1	0	0	1	0	1
2	0	1	0	1	1
3	0	1	1	1	0
4	1	0	0	0	1
5	1	0	1	1	1
6	1	1	0	1	0
7	1	1	1	1	0

Table 3 illustrates a potential TT for an approximate FA, featuring two alterations in the s column (rows i = 3 and i = 7) and one alteration in the c_o column (row i = 4). These adjustments modify the logical equations as follows:

$$s' = (a + b) \oplus c_{in} \quad (3)$$

$$c_o{}' = c_{in} + ab \quad (4)$$

With two outputs (s and c_o) and eight entries in the TT, feasible modifications were obtained, representing the complete range of potential approximate FAs that could be constructed. Every approximate FA can be distinguished by a unique 4-digit hexadecimal identifier, referred to as ID, which encodes the binary strings of s and c_o.

3.2. Voltage Over Scaling

VOS is a prevalent run-time approximation technique, extensively utilized in earlier studies to regulate dynamic power consumption in CMOS circuits. This is due to the quadratic reduction of switching power with the voltage supply. In instances of over-scaling, circuits are engineered to function optimally within standard conditions. Nonetheless, their energy consumption could be diminished through voltage over-scaling, which involves utilizing a lower power supply voltage that may occasionally result in erroneous outputs from the circuit.

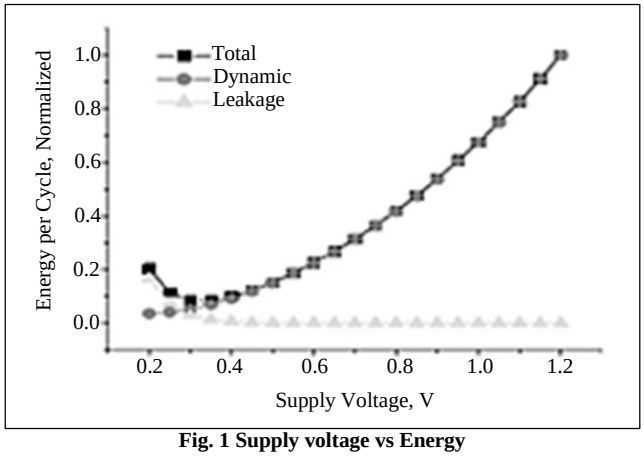

Fig. 1 Supply voltage vs Energy

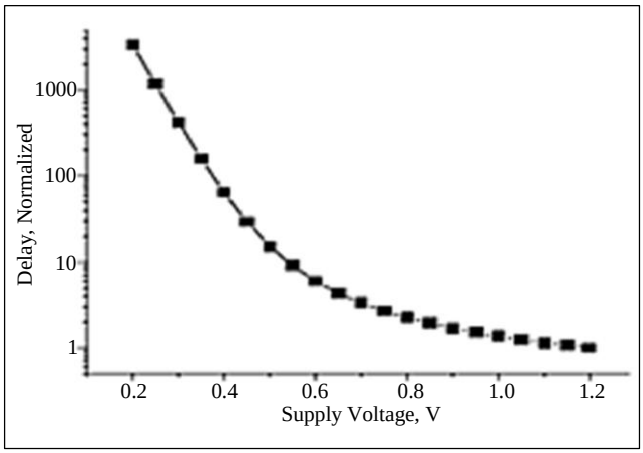

Fig. 2 Supply voltage vs Delay

VOS has been proven to effectively address strict power requirements and has been implemented in several designs. As shown in Figures 1 and 2 [32], when the supply voltage is reduced while maintaining a fixed threshold voltage, there is a quadratic decrease in dynamic energy, but with a trade-off of reduced performance. This decrease in performance may be acceptable for many applications. In fact, for a wide range of uses, such as sensors and medical devices, a significant decrease in performance may be acceptable without affecting the device's usefulness.

Additionally, high-performance designs can benefit from reducing the supply voltage during idle periods when the circuit is executing simple background routines, as the performance requirements are relaxed or eliminated. The use of VOS can result in significant energy savings whenever the performance requirements for a circuit are low, regardless of the application. Moreover, it is presented as a fault-tolerance technique [29] for realizing AxC by compromising limited accuracy and increasing circuit efficiency for image processing.

3.3. Gate Diffusion Input

GDI is a simple, low-power, and fast-to-develop technique that has been modified from a static CMOS design. Figure 3 shows the GDI cell, which consists of only two transistors suitable for digital combinatorial and sequential logic implementations. This simple structure provides reduced power consumption, delay, and area. Initially, GDI was developed for Silicon on Insulator (SoI) or twin-well CMOS fabrication process technologies but later used in CMOS fabrication process technology. The basic GDI logic appears similar to a static CMOS inverter; however, it differs in connecting the inputs [12], as discussed below:

- As shown in Figure 3, there are three input terminals and one output terminal; inputs terminals ‘P’, ‘N’ and ‘G’ are connected to the PMOS source, NMOS source and NMOS gate, as well as the PMOS gate, respectively.

Then, the output terminal 'OUT' is connected to the NMOS drain and the PMOS drain.

- The bulk of NMOS and PMOS were connected to GND and VDD, respectively.

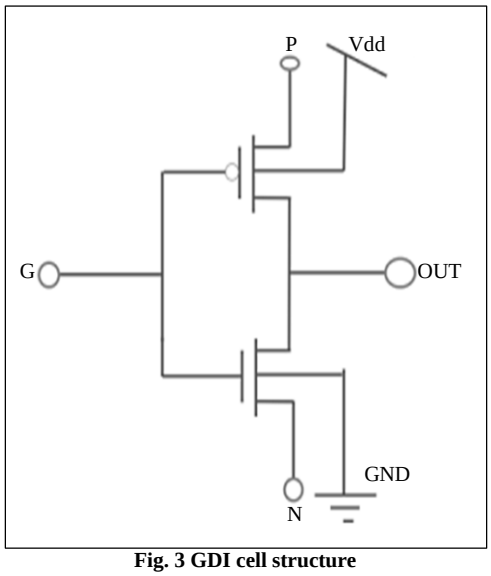

Fig. 3 GDI cell structure

Table 4. Truth table of GDI logic functions

N	P	G	Out	Function
0	B	A	$\bar{A}.B$	F1
B	1	A	$\bar{A}+B$	F2
1	B	A	$A+B$	OR
B	0	A	$A.B$	AND
C	B	A	$\bar{A}.B+A.C$	MUX
0	1	A	$\bar{A}$	NOT

Table 4 shows the truth table of GDI logic functions. The GDI construction, operation, transient analysis, output swing, switching functions and types are detailed in [12-19].

3.4. VOS-GAFA

This section presents the VOS-GAFA design. VOS-GAFA utilized the following strategies to achieve energy efficiency:

- Supply voltage scaled to 0.5V
- The GDI technique provides minimum power, delay, and area.
- Elimination of the carry logic part reduces area and power.
- Adder was designed using 14 transistors only.

The Boolean formulas for existing adders and proposed VOS-GAFA are displayed in Table 4. Full swing GDI-based OR, NOT, and MUX logic functions are used in VOS-GAFA. Figure 4 illustrates the suggested VOS-GAFA, which was created using just 14 transistors (14T) and with improved PMOS and NMOS widths. This circuit generates an output signal with full swing and complete adder functionality.

Table 5 presents the Boolean expressions for the Sum and Carry outputs of various existing approximate full adders, including the proposed VOS-GAFA. This table showcases the comparative simplification and design considerations of VOS-GAFA against other approximate adders. The NC-FET-CiM adder (approximate) produces the Sum output as 'B' and the Carry output as 'A,' indicating a simplified logic approach. The CNFET-AFA uses a more complex Sum equation and generates the Carry output.

The TACA-ACFA has a detailed Sum equation involving multiple terms, showing that it accounts for various input combinations for accurate approximation with the Carry output. The AA4 adder outputs a Sum based on a combination of AND and OR operations with A, B, and C inputs, while its Carry output is simply (A), reflecting a minimalistic design. Finally, the VOS-GAFA is designed with the Sum equation, highlighting the XOR-based logic for Sum calculation and the Carry output as (B), focusing on efficiency for resource-constrained applications.

Table 5. Boolean expressions for existing approximate full adders and VOS-GAFA

Adder Type	Sum	Carry	Ref
NCFET-CiM adder (approx)	$Sum = B$	$Cout = A$	10
CNFET-AFA	$Sum = \{B + (A + \bar{B})Cin\}$	$Cout = (B + Cin)A$	11
TACA-ACFA	$Sum = A \cdot B \cdot C_{in} + (A + B + C_{in}) \cdot (\overline{A + B})$	$Cout = A + B$	13
AA4	$Sum = (B\ AND\ C) + (\bar{A}\ AND\ C) + (\bar{A}\ AND\ B)$	$Cout = (A)$	16
VOS-GAFA	$\boldsymbol{Sum = (A\ XOR\ B)CIN + (\overline{A\ XOR\ B})\overline{CIN}}$	$\boldsymbol{Cout = (B)}$	**Proposed**

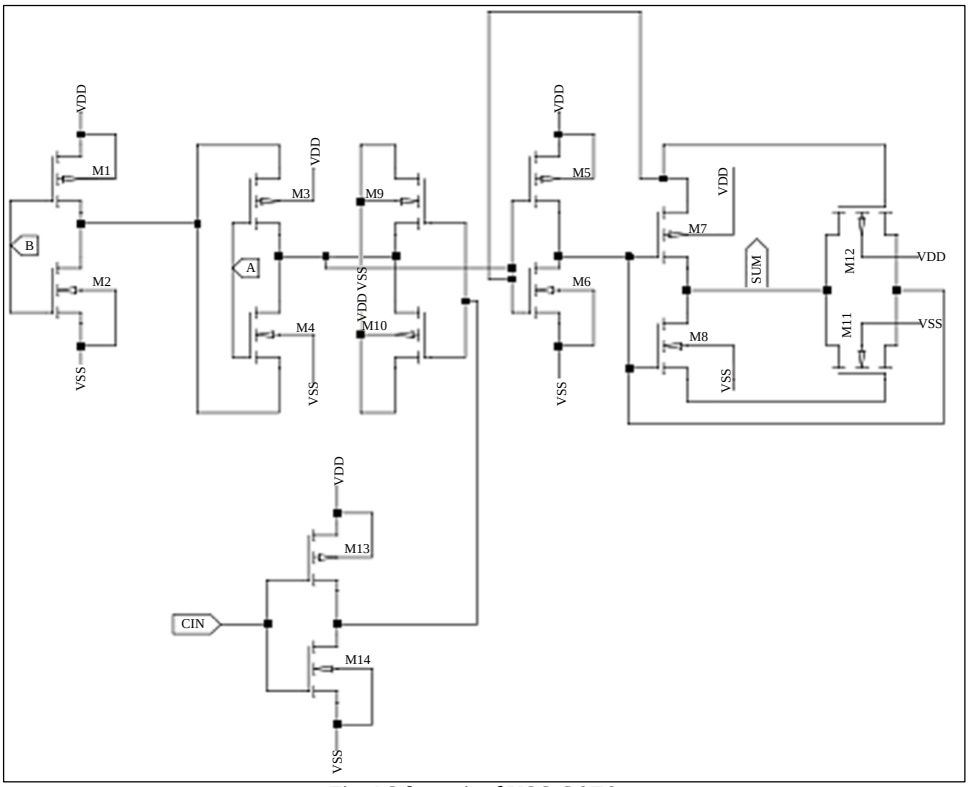

Fig. 4 Schematic of VOS-GAFA

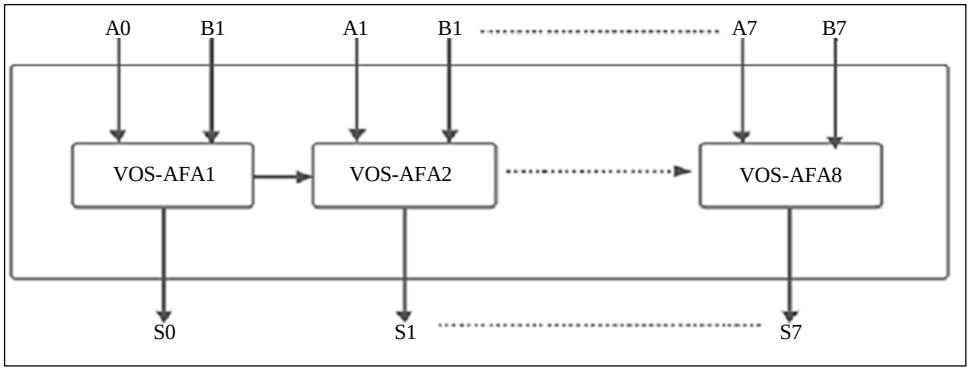

Fig. 5 Structure of VOS-RCA

The schematic diagram represents the VOS-GAFA circuit, designed to optimize power consumption and transistor count for resource-constrained applications. The circuit uses GDI technique transistors, where M1, M2, M3, and M4 form the initial input section for generating partial sum outputs. Transistors M9 and M10 are configured to assist with VOS and logic propagation. M5 through M8 form the carry-out generation section, where transistors M7 and M8 work to ensure proper logic levels for the carry output, leveraging VOS to save power. Additionally, M11 and M12 are used to strengthen the signal and improve the Noise Margin (NM), enhancing robustness against noise. The carry-in input is handled by transistors M13 and M14, which are configured to allow for minimal delay and efficient VOS. The integration of these components ensures a balance between reduced transistor count and improved noise tolerance. Figure 5 shows the block diagram of 8-bit RCA using VOS-GAFA, known as VOS-RCA.

The schematic diagram illustrates the 8-bit VOS-RCA, constructed using eight instances of the VOS-AFA blocks labeled as VOS-AFA1 through VOS-AFA8. Each VOS-AFA block adds a corresponding pair of input bits (A0, B0 through A7, B7) and produces an output sum (S0 through S7). The carry output of each VOS-AFA block propagates sequentially to the next adder block, creating a ripple effect for the carry signal across the chain of adders. This VOS-RCA design utilizes approximate full adders to reduce power consumption and enhance speed, utilizing the VOS approach to optimize performance for power-sensitive applications.

4. Results and Discussion

4.1. Experimental Setup

The proposed VOS-GAFA and VOS-RCA are developed in a cadence virtuoso atmosphere with gpdk45nm technology. First, the schematics and symbols were developed using virtuoso editors, and then the test bench was created for simulation, as shown in Figure 6.

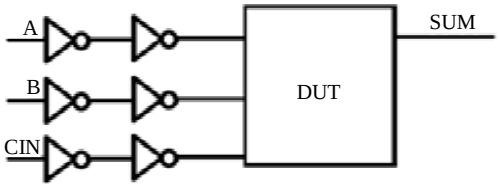

Fig. 6 Simulation test bench

The delay depends on circuit topology, technology, and input signal slope. Hence, to obtain the realistic input slope, the input signals A, B and CIN are passed through buffers, as shown in Figure 6. The input signal frequency was taken up to 50 MHz with the supply voltage scaled to 0.5 V. The average power (Pavg) and propagation delay (Tpd) were calculated from the transient analysis, and the noise margin was calculated from the DC analysis. The proposed adders have been simulated in all the process corners (SS, FF, FS, SF and TT), and the Worst-case process corner results are selected for comparison with existing adders to ensure that the proposed adder operates in typical operating conditions.

4.2. Simulation Results

The transient simulation is shown in Figure 7. Tables 6 and 7 represent the results of the 1-bit and 8-bit FA. Table 8 shows the VOS-GAFA power, delay, PDP, and transistor count results of VOS-GAFA. The high noise margin (NM_H) and low noise margin (NM_L) are given in Equations (1) and (2) respectively,

$$NM_H = V_{OH} - V_{IH} \tag{5}$$

$$NM_L = V_{IL} - V_{OL} \tag{6}$$

From Equations (3) and (4), the calculated NMH and NML of VOS-GAFA are 191.12mV and 204.04mV. Since both values are higher, the VOS-GAFA circuit provides proper operation and robustness against noise sources. The 8-bit VOS-RCA is designed using VOS-GAFA in a Ripple Carry adder (RCA) structure. Figure 8 shows the simulation waveform. Figure 9 represents the schematic representation of a 1-bit FA circuit. Figure 10 represents the schematic representation of the 1-bit FA test circuit. Figure 11 shows the schematic representation of the 8-Bit RCA Circuit. Figure 12 shows the simulation results of the VOS-GAFA model.

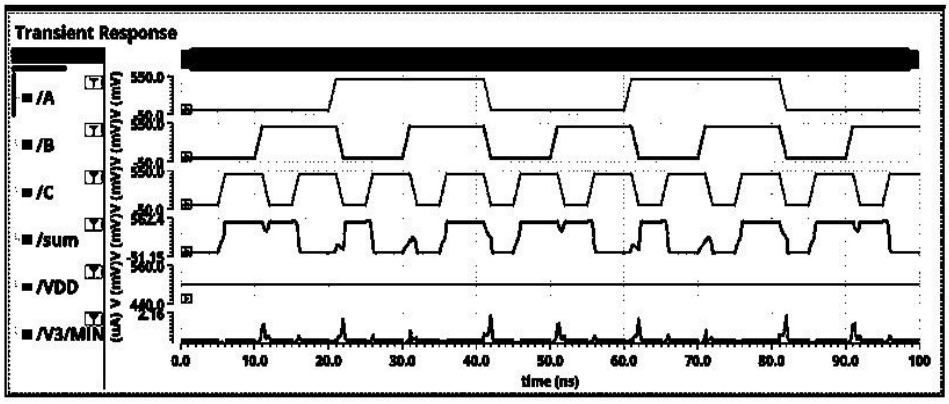

Fig. 7 Simulation output of VOS-GAFA

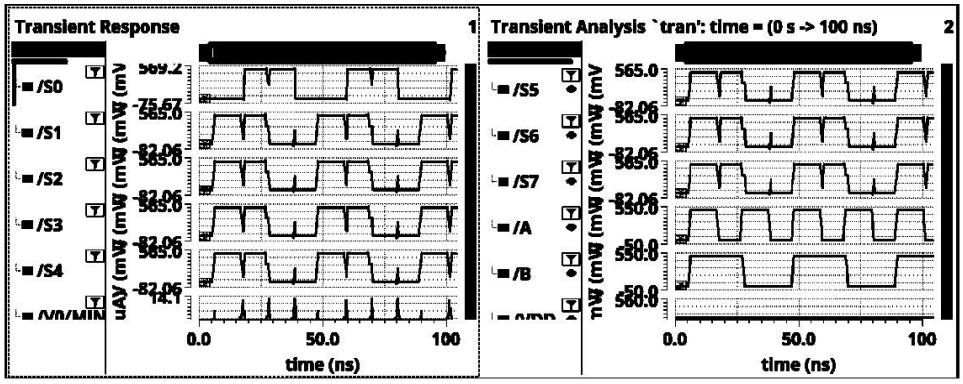

Fig. 8 Simulation output of VOS-RCA

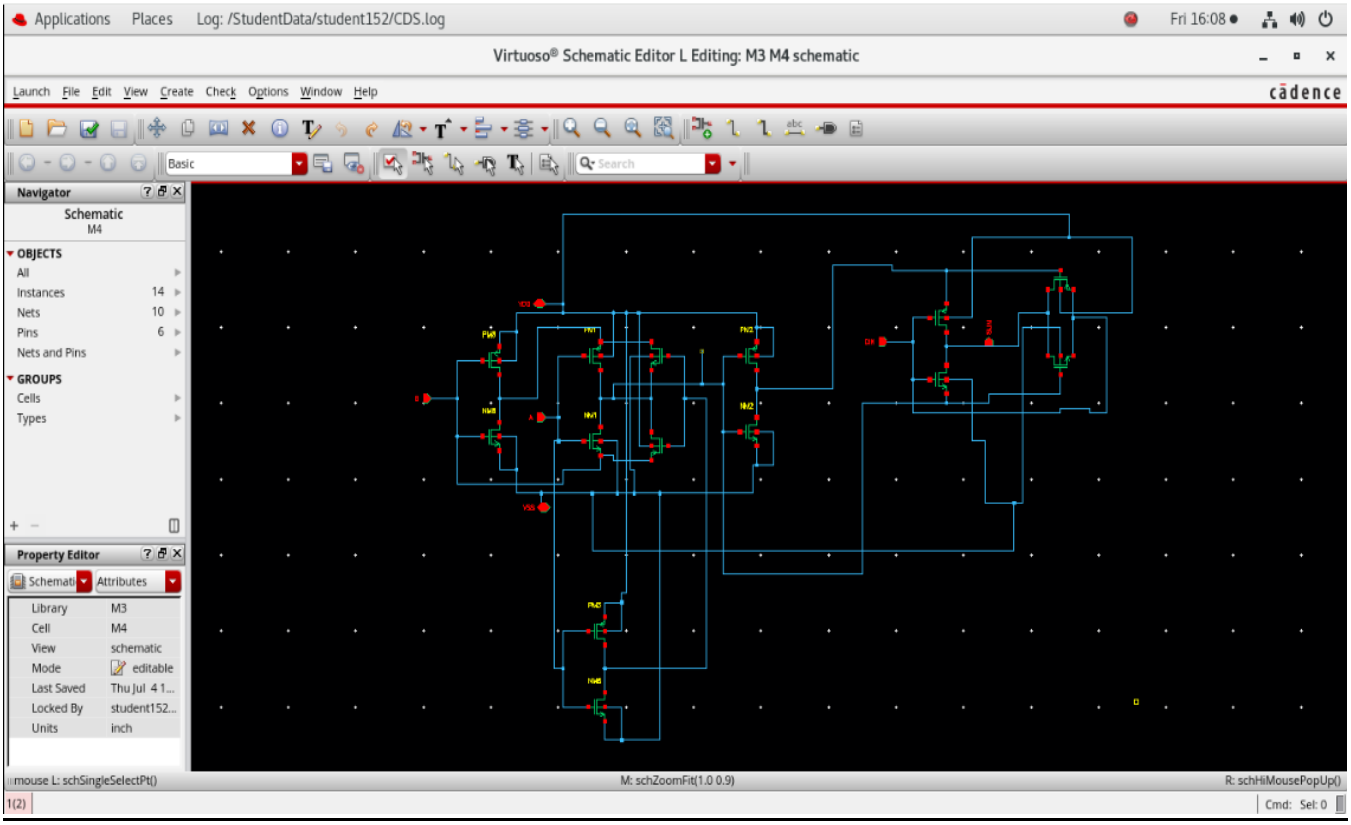

Fig. 9 Schematic of 1-Bit FA circuit

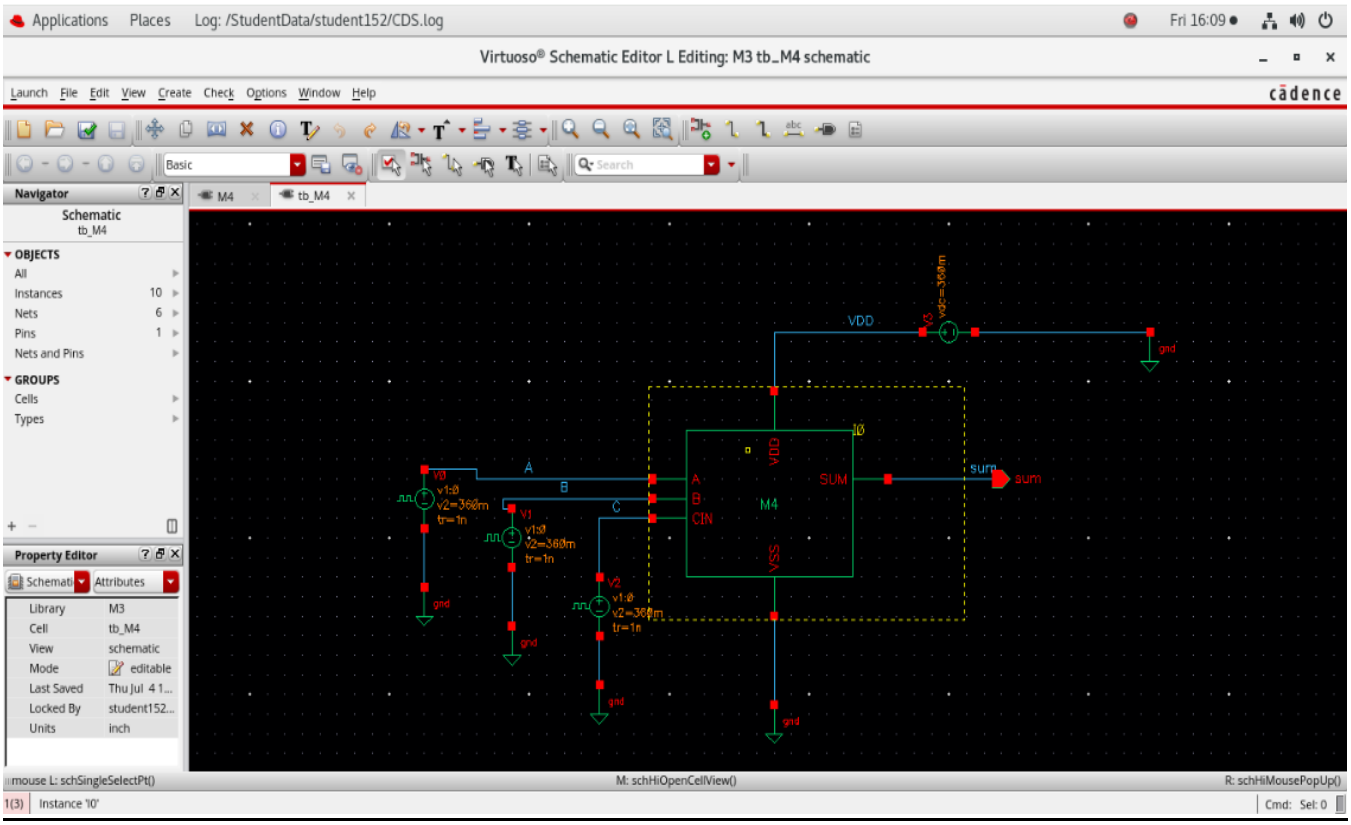

Fig. 10 Schematic of 1-Bit FA test circuit

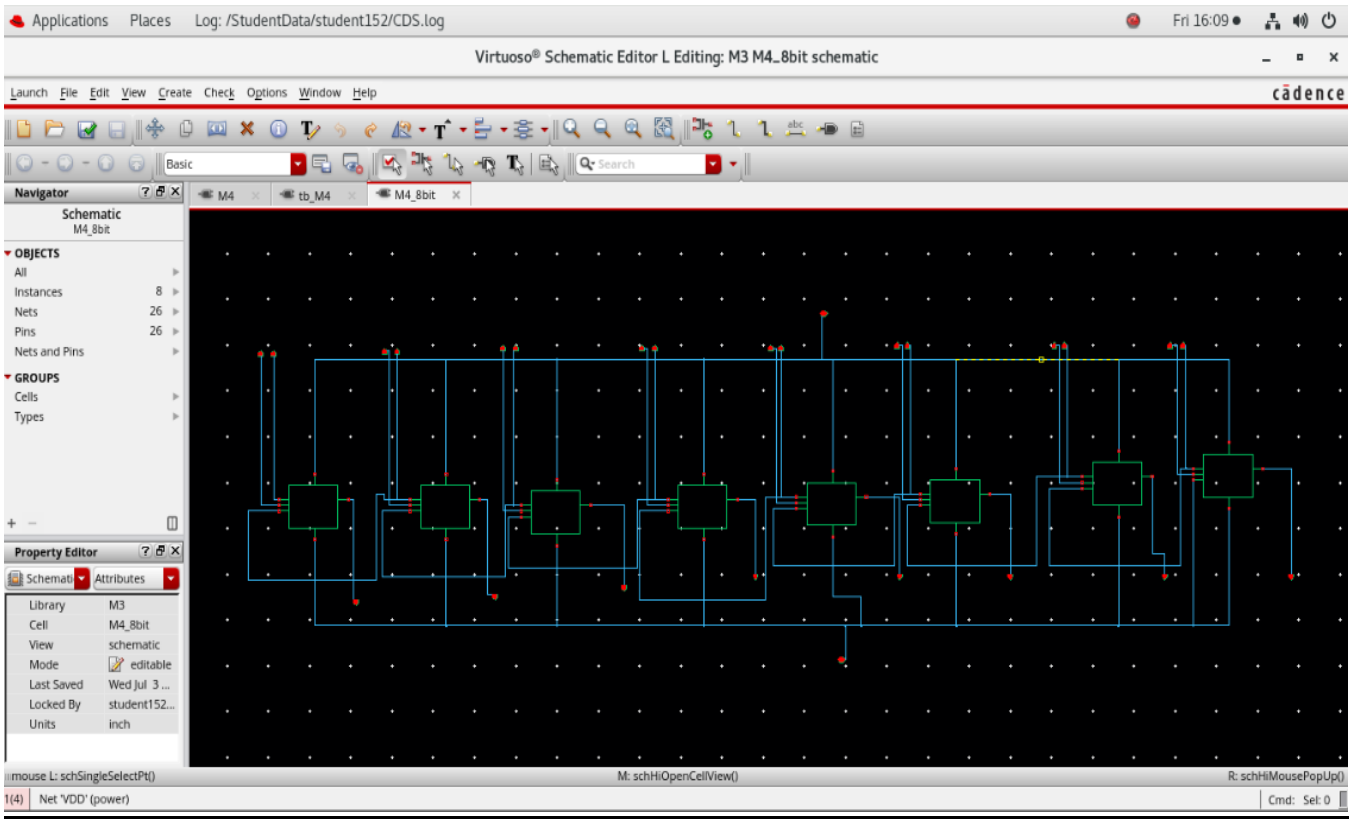

Fig. 11 Schematic of 8-Bit RCA circuit

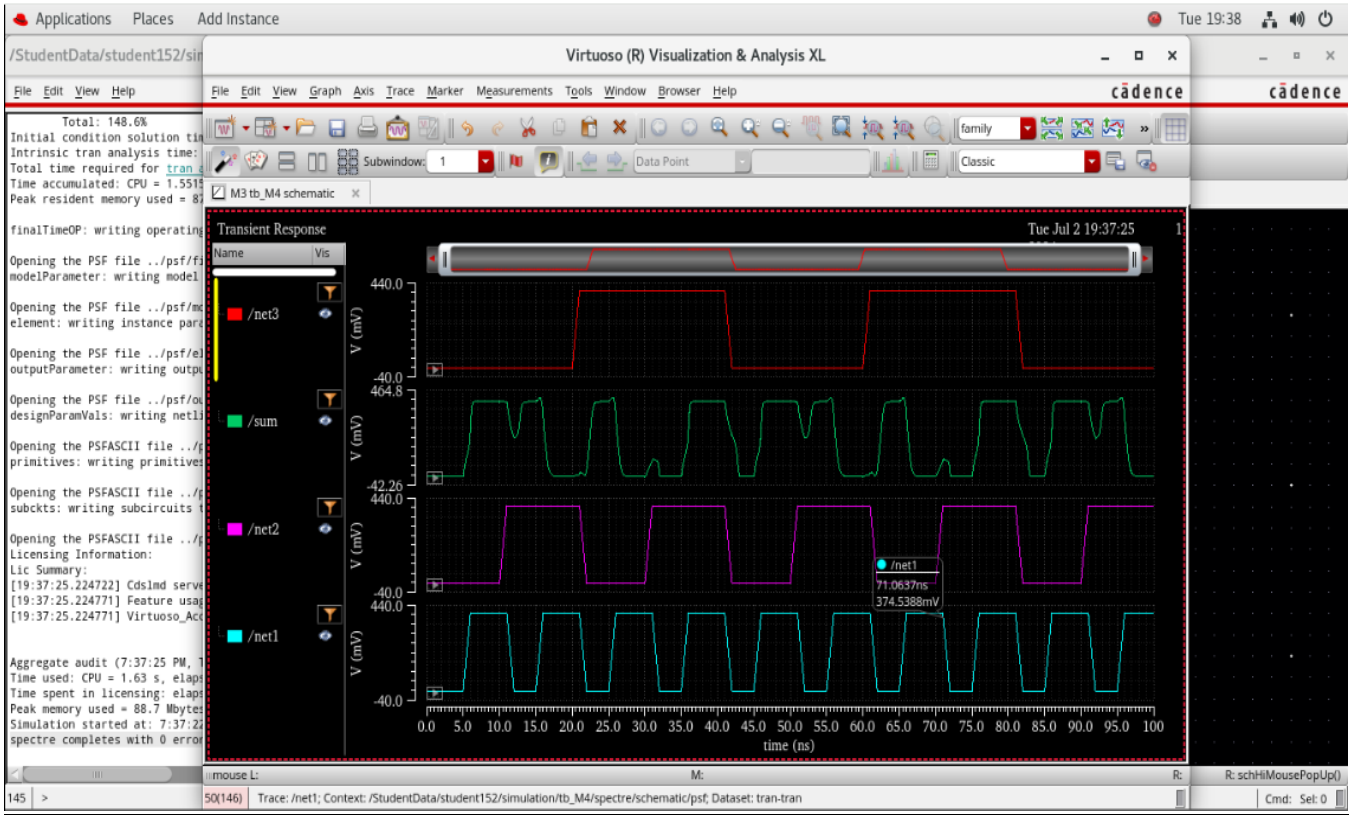

Fig. 12 Simulation results of VOS-GAFA

Table 6. Results of 1-bit full adder comparison

Adder Type	Average Power	Delay	PDP	Transistor Count	Tech Node	Tech	VDD
NCFET-CiM Adder [10]	58n	200p	0.0116f	25	40nm	CMOS	0.5V
CNFET-AFA [11]	660n	3100p	2.046f	8	32nm	CNFET	0.5V
AA4 [16]	50.9p	181500p	9.25f	14	45nm	CMOS	0.5V
TACA -ACFA [13]	18.8n	478.2p	0.009	32	SMIC 40nm	bulk CMOS	0.5V
Proposed Model	25.451n	532.629p	0.0135f	14	45nm	bulk CMOS	0.5V

Table 7. Results of 8-bit full adder comparison

Adder Type	Average Power	Delay	PDP	Transistor Count	Tech Node	Tech	VDD
CNFET-AFA [11]	6442.6n	32308p	208.147f	82	32nm	CNFET	0.5v
AA4 [16]	1.82p	5.12n	4.64E-18	NA	45nm	CMOS	0.5V
TACA -AM [13]	18.820n	478.20p	0.009f	NA	SMIC 40nm	CMOS	0.5V
Proposed Model	219.027n	932.734p	0.2042f	112	45nm	CMOS	0.5V

Table 8. Simulation results of existing approximate full adders and VOS-GAFA

Adder Type	Power (nW)	Delay (ps)	PDP (fW-s)	Transistors Count
NCFET-CiM [10]	58	200	0.0116	25
CNFET-AFA [11]	660	3100	2.046	8
TACA -ACFA [13]	18.8	478.2	0.009	32
AA4 [16]	0.050	181500	9.25	14
VOS-GAFA	25.451	532.629	0.0135	14

4.3. Performance Evaluation

Table 9 provides a comparison of the power consumption and delay for the proposed full adder circuit (VOS-GAFA) under different process corners, labeled as typical-typical (tt), slow-slow (ss), fast-fast (ff), fast-slow (fs), and slow-fast (SF). These process corners represent variations in fabrication conditions that can impact the circuit's performance. The power consumption ranges from 18.9274 nW (in the sf corner) to 25.451 nW (in the ff corner), demonstrating relatively low power requirements, which is advantageous for energy-efficient applications.

Delay, a measure of the time taken for signal propagation, varies significantly across process corners, with the lowest delay of 183.578 ps observed in the ff corner and the highest delay of 532.629 ps in the ss corner. This variation in delay reflects how different fabrication conditions can impact speed, with faster corners (ff) offering quicker responses and slower corners (ss) resulting in increased delay. Figure 13 shows the graphical plot of FA's power and delay comparison.

Table 9. Full Adder's power and delay comparison

Process Corners	Power(nW)	Delay (ps)
tt	19.2826	337.288
ss	19.2354	**532.629**
ff	**25.451**	**183.578**
fs	22.1485	275.791
sf	**18.9274**	378.082

Table 10 compares the power consumption and delay of the proposed 8-bit VOS-RCA across different process corners: tt, ss, ff, fs, and sf. The power consumption varies from 173.046 nW in the sf corner to 219.027 nW in the ff corner. This indicates that the VOS-RCA maintains relatively low power usage, with minor fluctuations depending on fabrication conditions.

Delay, representing the time required for the carry to propagate through the entire 8-bit adder, ranges from 787.934

ps in the ff corner to 932.734 ps in the sf corner. This variability reflects how different process conditions impact the adder's performance, with faster corners (ff) achieving lower delay and slower corners (sf) leading to higher delay.

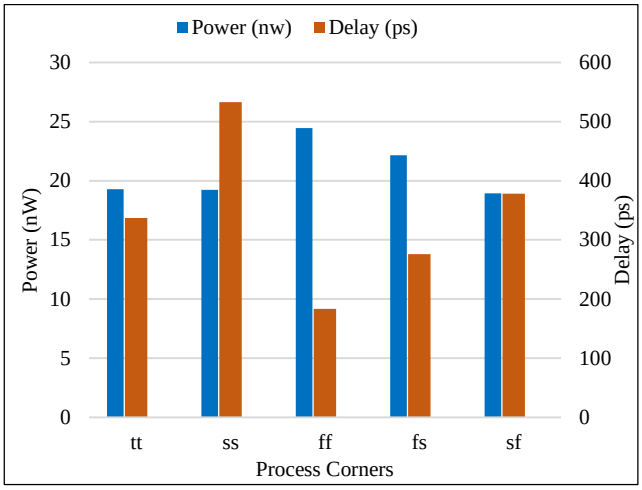

Fig. 13 Comparison of FA's power and delay consumption

Table 10. Ripple Carry Adder's power and delay comparison

Process Corners	Power(nW)	Delay (ps)
tt	189.004	874.147
ss	177.679	**867.219**
ff	**219.027**	**787.934**
fs	208.78	857.4
sf	**173.046**	**932.734**

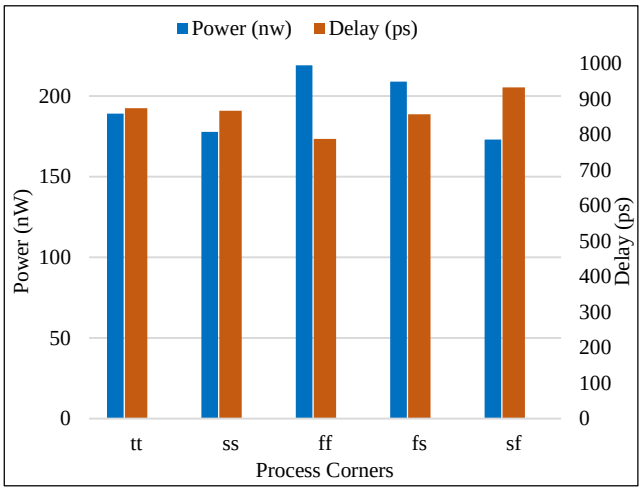

Fig. 14 Comparison of RCA's power and delay consumption

Figure 14 shows the graphical plot of RCA's power and delay comparison. Table 8 summarizes the simulation results of various existing approximate FAs and the proposed VOS-GAFA, comparing their power consumption, delay, Power-Delay Product (PDP), and transistor count. The NCFET-CiM adder has a power consumption of 58 nW and a delay of 200 ps, yielding a PDP of 0.0116 fW-s with 25 transistors. The CNFET-AFA demonstrates significantly higher power and delay values at 660 nW and 3100 ps, respectively, with a high PDP of 2.046 fW-s but only 8 transistors.

The TACA-ACFA consumes 18.8 nW with a delay of 478.2 ps, resulting in a PDP of 0.009 fW-s, albeit using 32 transistors. The AA4 adder has minimal power consumption (0.050 nW) but an extremely high delay (181500 ps), leading to a high PDP of 9.25 fW-s with 14 transistors. In comparison, the proposed VOS-GAFA achieves a balance, with moderate power consumption (25.451 nW) and delay (532.629 ps), yielding a PDP of 0.0135 fW-s and a transistor count of 14. These results indicate that VOS-GAFA provides an efficient trade-off in power, delay, and transistor count. It is suitable for low-power applications in IoT edge and fog computing, where energy efficiency is crucial.

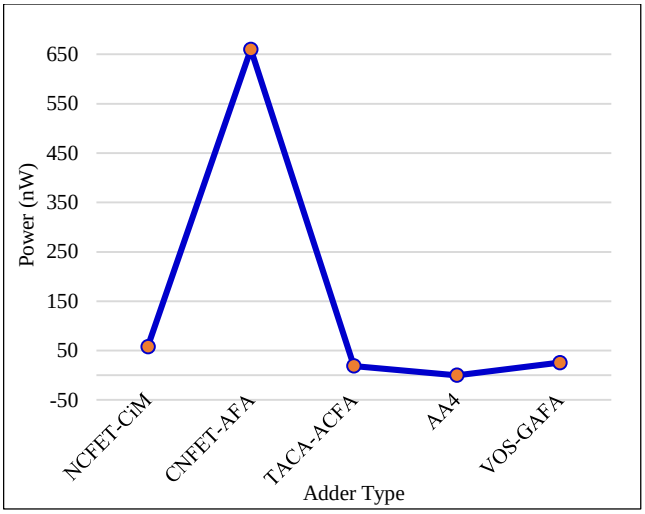

Fig. 15 Comparison of power consumption

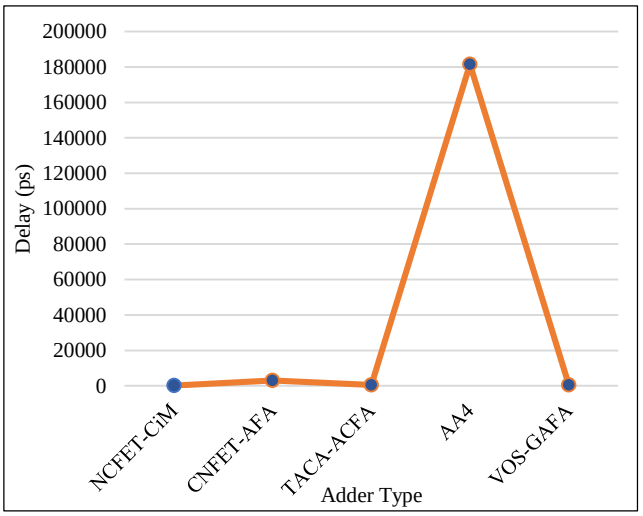

Fig. 16 Comparison of delay

Figures 15 to 18 show the results of a comparison of the existing approximate full adder and proposed VOS-GAFA, respectively. From Figure 15, it is noted that the proposed VOS-GAFA offers outstanding power characteristics with ultra-low power consumption, whereas CNFET-AFA has high power consumption. As observed from Figure 16, AA4 has a very high delay, CNFET-AFA offered a moderate delay, and at the same time, the proposed VOS-GAFA achieved very little delay. CNFET-CiM has the worst PDP among all existing adders, whereas the proposed VOS-GAFA offers a competitive PDP value, as shown in Figure 17. From Figure 18, NCFET-CiM and TACA-AM have very high transistor counts of 25 and 32, respectively, whereas the proposed VOS-GAFA has a competitive transistor count among all existing approximate full adders.

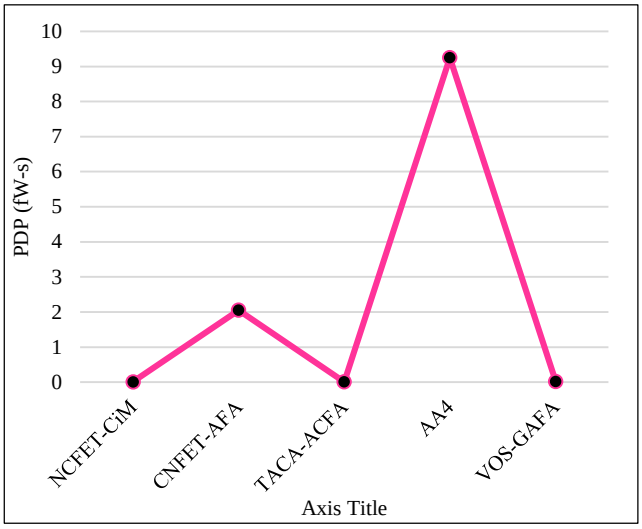

Fig. 17 Comparison of PDP

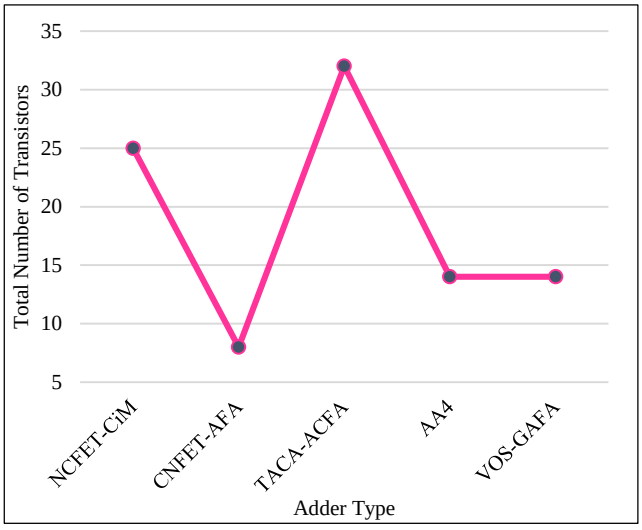

Fig. 18 Comparison of transistor count

This comparison points out that the existing approximate full adders have reduced efficiency, at least in any performance metrics (power, delay, and transistor count). This makes the existing adder's advantages become obsolete. On the other hand, the proposed VOS-GAFA achieved ultra-low power consumption, less delay, competitive PDP, and transistor count. The VOS-GAFA power consumption and transistor count are reduced by 56.11 % and 44%, respectively, when compared with the best existing technique. Next, the 8-bit VOS-RCA performance is compared with 8-bit CNFET-RCA [11]. From the simulation results, VOS-RCA has achieved improvement in power, delay, and PDP at the cost of 25.7% increased transistor area.

The VOS-RCA and VOS-GAFA hold significant potential in various existing and emerging technologies due to their optimized power, delay, and PDP characteristics. In wearable devices and smart sensors, these adders can be employed to enhance energy efficiency and performance, enabling prolonged battery life and real-time processing capabilities for health monitoring and activity tracking. Additionally, in edge computing for IoT applications, VOS-RCA and VOS-GAFA can support low-power and high-speed data processing for smart home systems, autonomous vehicles, and industrial automation. Their ability to operate efficiently under VOS makes them ideal for error-tolerant applications such as multimedia processing, image and video encoding, and neural network computations, where power savings and speed are critical without compromising acceptable output accuracy.

The VOS-RCA and VOS-GAFA designs demonstrate significant potential for robust performance in extreme scenarios typical of IoT applications. Under low-power constraints, these designs maintain energy efficiency while delivering acceptable computation accuracy, making them suitable for energy-harvesting IoT devices. In scenarios with fluctuating supply voltages or noisy environments, the VOS technique ensures reliable operation with tolerable errors. For high-throughput edge devices, such as those processing real-time data in smart cities or industrial IoT, the adders' low-delay characteristics ensure minimal computational bottlenecks. Additionally, in temperature and process variation-sensitive environments, such as wearables or remote sensors deployed in harsh conditions, the transistor-level optimizations of VOS-RCA and VOS-GAFA enable stable operation. However, further resilience testing and adaptive error mitigation strategies could enhance their robustness for mission-critical IoT applications.

4.4. Advantages and Limitations

The VOS-GAFA model achieves superior results compared to state-of-the-art techniques due to its integration of VOS and GDI technology, which synergistically enhances power efficiency and circuit simplicity. By leveraging VOS, the model operates at reduced supply voltages, effectively minimizing power consumption while maintaining acceptable levels of computational accuracy in error-tolerant scenarios.

The GDI technique further optimizes the design by reducing the transistor count, which not only lowers power consumption but also minimizes circuit complexity and area. Unlike traditional adders, which often involve higher transistor counts and PDP, VOS-GAFA strikes an ideal balance between power, delay, and robustness. The high noise margin in VOS-GAFA ensures stable operation under noisy conditions and voltage fluctuations, outperforming other approximate full adders that suffer from significant trade-offs between power efficiency and reliability.

The VOS-GAFA and VOS-RCA designs offer several advantages, including significant reductions in power consumption and transistor count, making them highly energy-efficient for resource-constrained IoT and edge computing devices. Their low PDP ensures optimal performance in real-time applications, and the high noise margin enhances operational robustness against environmental and circuit noise.

Furthermore, their suitability for error-tolerant applications expands their usability across diverse domains like multimedia processing, neural network computations, and wearable devices. However, the designs have limitations, such as potential accuracy trade-offs under extreme VOS, which may restrict their application in precision-critical tasks. Additionally, their performance needs further evaluation in large-scale systems and under diverse real-world conditions, including temperature and process variations, to fully assess their scalability and reliability in more complex computational environments.

5. Conclusion

In this work, VOS-GAFA is designed at the transistor level using gpdk45nm technology. All the designs are developed in the cadence virtuoso suite and simulated using a spectre simulator. The experimental results of the proposed VOS-GAFA have shown 56.11 % and 44 % reduction of power consumption and transistor count, respectively, when compared to the best existing approximate full adder. Moreover, VOS-GAFA has a high Noise Margin (NM) value that provides proper circuit operation and robustness against noise sources. VOS-RCA showed improved power, PDP, and delay values when compared to existing 8-bit RCA, and hence, it is appropriate for resource-constrained edge and fog IoT devices. From the experimental results, VOS-GAFA consumes ultra-low power, less delay, competitive PDP and moderate transistor count.

The high noise margin of VOS-GAFA guaranteed proper circuit operation and robustness. Also, VOS-RCA provided improved power, delay and PDP by sacrificing an increased area of 25.7%. Hence, the proposed adder can be deployed in edge and fog IoT devices and other applications. In the future, this research can focus on further optimizing the VOS-RCA and VOS-GAFA for ultra-low-power applications by exploring advanced transistor technologies such as Tunnel FETs and FinFETs.

Additionally, integrating these adders into larger computational architectures like multipliers or digital signal processors can be explored to evaluate their scalability and performance in complex systems. Extending their application to machine learning accelerators and edge AI frameworks can provide insights into their efficiency in data-intensive tasks. Moreover, research can investigate adaptive voltage scaling techniques and hybrid error-correction mechanisms to enhance their applicability in safety-critical domains, such as autonomous systems and healthcare devices.

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